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Detailed Description of Clock and Sync

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1 Introduction

1.1 Purpose of this document

This document provides the overall description of the clock subsystem for the LOFAR stations. More detailed information on the different parts of the clock subsystem can be found in the relevant product specifications/product descriptions and the SCO-LCU interface description document.

1.2 References

[1] Clock Distribution Performance Requirements, LOFAR-ASTRON-SER-016, v1.1
[2] Remote Station Clock and Synchronization, LOFAR-ASTRON-MEM-154 v0.6
[3] LOFAR System Requirements Specification, LOFAR-ASTRON-SRS-001, v3.0
[4] Station Systems Architectural Design Document, LOFAR-ASTRON-ADD-013, v1.0
[5] Description of the Control Interface between SCO and LCU/RSP, LOFAR-ASTRON-RPT-051, v0.2
[6] Critical Evaluation of the Motorola M12+ GPS Timing Receiver vs. the master clock at the United States Naval Observatory, Washington, DC, R.M. Hambly and T.A. Clark, 34th Annual Precise Time and Time Interval (PTTI) Meeting
[7] Manuals for the GPS and Rb-reference standard for FTS-2, LOFAR-ASTRON-MAN-013, v0.1
[8] Subrack Specifications, LOFAR-ASTRON-MEM-196 1.0

1.3 Abbreviations

COTS	Commercial of Shelf
FTS-2	Final Test Station 2
GPS	Global Positioning System
LCU	Local Control Unit
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor to Transistor Logic
PA	Power Amplifier
PECL	Positive Emitter Coupled Logic
PPS	Pulse Per Second
RSP	Remote Station Processing board
Rb	Rubidium
SCO	Station Clock
TDS	Timing Distribution board Subrack

1.4 Glossary

LVPECL Low Voltage PECL is a 3.3V standard where the reference level is defined as the supply voltage -1.3V, so for a 3.3V supply, this is 2V. The swing around this reference level is 800mV for a reasonable termination resistance and a low switching speed.

LVTTL Low voltage TTL is a standard based on a 3.3V power supply where zero's and one's are coded as below 10% of the supply voltage and above 90% of the supply voltage

2 Requirements

2.1 Performance requirements

There are two requirements identified on the clock system:

1. The clock stability should not influence the measurements results in relation to the inaccuracies introduced by the rest of the LOFAR system and the characteristics of the measurement environment. A performance requirement analysis has been done on those parts of the system deemed relevant for the clock stability, see [1]. At the same time, a basic design of the clock system was made and the essential components were selected which were considered a good compromise between cost and performance.

2. All AD-converters should sample synchronously. It is assumed that an offset (in station time) of less than 200ps does not impact the performance as long as the offsets are stable over time.

After careful consideration, the performance requirements on the LOFAR clock system were split into three groups.

2.1.1 Start-up Requirements

During Start-up, the time difference between the different stations needs to be identified. This can be done based on the time stamp of the PPS at the lowest specified receive frequency, 30MHz if an instantaneous offset of half a wavelength is allowed, than the maximum error between two PPS signals shall be less than 16ns.

Also at Start-up, the clock system shall provide a clock of 200MHz to the RSP boards.

The TDS boards do not have any self configuration capabilities; therefore the RSP board shall be able to program the TDS boards via I2C.

After a cold (re)start, the clock system shall be stable within 6 hours. With the current settings for the Rubidium reference, 6 hours is the time needed to reach a stable situation.

After a cold (re)start, the 160/200MHz PLL shall be locked in less than one second.

2.1.2 Time Dependent Requirements

The time dependent requirements specify how the different clock signals behave over time.

The time between two subsequent PPS signals to the RSP board shall be 1s with a maximum error of 5ns, thereby assuring that exactly 160/200Msamples/s are taken between two PPS signals.

The RSP board shall inform the LCU if there are more, or less, than 160/200Msamples in one second.

The reference clock shall have an Allan variance of 1e-11 or less over 10s.
Note: The ionosphere has a variation of 0.8e-11 over 10s.

The RMS jitter of any 160/200MHz signal to the RCU's or RSP boards shall be less than 1ps.
Note: This requirement seems to be sufficient with respect to the overall system performance.

2.1.3 Space Dependent Requirements

The space dependent requirements specify the performance of the distribution of a single clock flank to all AD converter clock inputs.

The time difference between two clock flanks distributed to two different RCU's within a station shall be less than 200ps before calibration

The instantaneous difference between two GPS PPS signals shall be less than 100ns
Note: as specified by the Motorola chipset

The RMS difference between two station PPS signals shall be less than 16ps

2.2 Mechanical/Electrical requirements

The Mechanical and Electrical requirements describe the physical sizes of all parts of the clock system and the internal/external interfaces of the different boards/units

2.2.1 Mechanical and Electrical requirements for the TDS board

De Mechanical and Electrical requirements for the TDS boards are closely related to the implementation of the Subrack described in [8]. The TDS board shall have front connectors for the PPS signal and for the 10MHz signal.

2.2.2 Mechanical and Electrical requirements for the GPS/Rb-reference

The combination of GPS/Rb-reference shall be mounted in a standard 19" rack with a maximum height of 3U

The combination of GPS/Rb-reference shall be provided with 230V AC power

The GPS antenna shall be mounted in such a way that it has a clear view of the sky for elevations larger than 10°.

The cable between the GPS receiver and the GPS antenna shall comply with the relevant requirements of the manufacturer.

2.2.3 Cabling

All cabling of the clock system shall be installed according to the guidelines provided by the cable manufacturer.

The cable delay between the GPS antenna and GPS receiver shall be measured with an accuracy of better then 1ns
Note: The Motorola GPS receiver can compensate for the length of the cable in 1ns steps.

The cable delay between GPS receiver and the Rubidium Reference receiver shall be measured with an accuracy of better then 1ns
Note: The FS-725 Rubidium reference can compensate for the length of the cable in 1ns steps

The cabling between the Rubidium reference and the TDS clock boards shall have equal electric length with accuracy of better than 0.25ns (approximately 4cm, estimated cable length: 7m).

2.3 External interfaces

Here the interfaces from the clock system to other parts of the LOFAR system are defined.

- The 160/200MHz clock signal to the RCU and RSP boards shall be based on the PECL standard.

- The PPS signal from the TDS board to the RSP board shall be based on LVTTL.
- The TDS board shall provide a visual indication of its status on the front panel.
- The combination of GPS/Rb reference shall provide a visual indication of its status.
- The GPS/Rb-reference shall be controlled from the LCU with an RS-232 interface.
- The PPS signal from the GPS/Rb reference shall be provided to the LCU on pin 1 of the RS-232 interface.
- The GPS receiver shall comply with the relevant GPS standards.
- The interfacing from the clock system to non-astronomical systems shall be based on the NTP protocol.
- The interface between the clock system and the LCU is described in more detail in [5]

2.4 Operation and Maintenance Requirements

The O&M interface can be found in [5]. In this section the requirements are summarized.

- The TDS board shall be programmable via de I2C interface to the backplane.
- The TDS board shall have an onboard connector I2C for configuration and testing purposes.
- The PLL lock status from each TDS board shall be accessible from the LCU.

3 Clock Architecture

The Clock Architecture is split into three distinct parts, the clock distribution between stations, the clock distribution within a station and the control architecture for the clock system within a station. This paragraph is based on the information in [1], [2] and [4].

3.1 Clock distribution between stations

3.1.1 Solution for LOFAR Stations

The distribution of the clock between stations is based on the PPS signals from the GPS system. The GPS system is the most widely used system to distribute a common reference clock to a large numbers of sites.

The PPS from the GPS receiver is used to discipline an Rb-reference standard (SRS-FS725). The GPS provides the LCU with the UTC-time, provided al correction factors (cable lengths, etc) are entered correctly. The LCU is also provided with the PPS signal from the SRS-FS725 which is used as the time reference for each station. This is possible because the output PPS of the SRS-FS725 is aligned with the input PPS (which is the GPS output). The UTC-time is encoded into a second counter which is sent to CEP together with the measurement data. The interconnection between the different units is shown in Figure 1

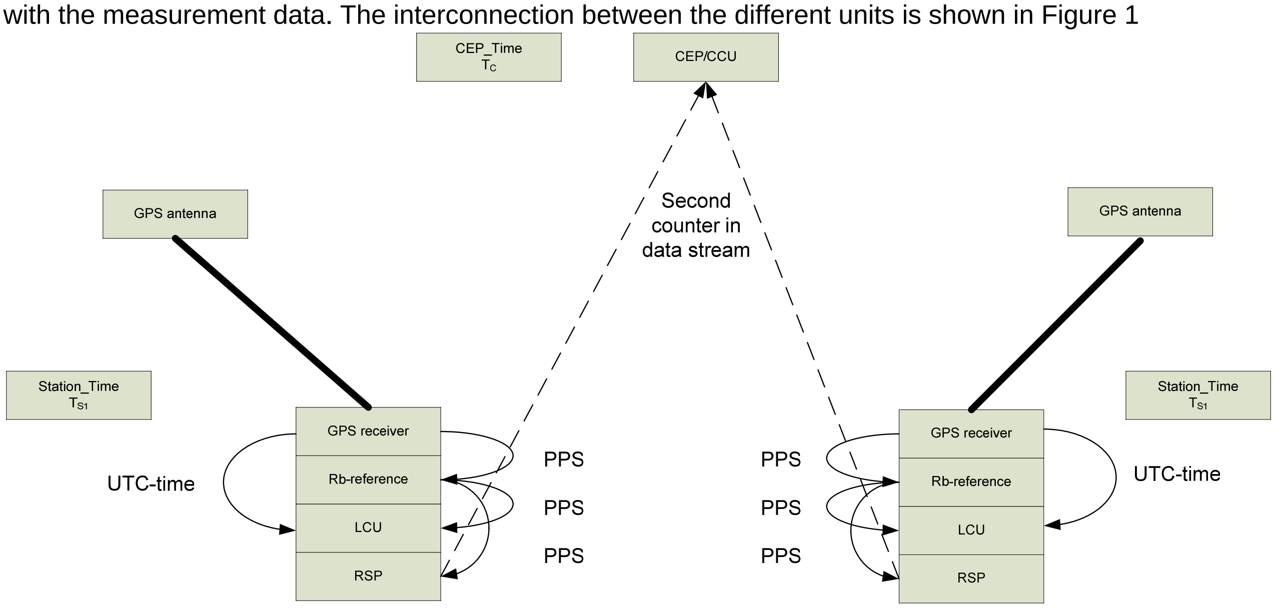

Figure 1, distribution of the UTC reference time through the LOFAR system

The Rb-reference (SRS-FS725) also provides a 10MHz reference signal which is locked to the PPS output signal.

For the Motorola M12 chipset was chosen because the specified offset from GMS of <50ns in timing mode was sufficient to instantaneously measure the offset between stations at a receive frequency of 10MHz. The RMS offset of <2ns 1sigma value was sufficient to also determine time difference at higher frequencies when using averaging.

3.1.2 Solutions for LOFAR roll-out

Motorola has stopped accepting orders for their GPS modules, improved modules are available by i-LOTUS, the M12M or integrated the Synergy Systems LLC, SynPaQ III GPS Sensor Timing Receiver w/M12M

3.1.3 Other investigated alternatives

3.1.3.1 Galileo

The Timing information from the Galileo system together with a crystal oscillator or Rb-reference standard could be used to generate the station time. The advantage of Galileo compared to GPS is that in theory, Galileo can provide a better time accuracy.

3.1.3.2 NTP via the control network

The use of the Network Timing Protocol (NTP) has been investigated but measurements performed by different institutes indicate that the timing accuracy over a controlled network was in the order of microseconds. The difference between the requirement and the expected accuracy is too large to further consider this method.

3.1.3.3 Crystal Oscillator (OCXO) instead of a SRS-FS725 Rb-reference standard

Some Crystal Oscillators have the advantage that they have a better Allan variance for periods of up to 10s and therefore it can be claimed that they have a better performance than the SRS-FS725 Rb-reference standard. The performance for time periods above 10s, the SRS-FS725 performs better. Therefore choosing an OCXO would require a maximum calibration interval of 10s and it would require a significantly better GPS (or GALILEO) receiver because de Rb-reference is used to average the PPS signal from the GPS receiver thereby making it possible to identify the time difference between stations at receive frequencies above 10MHz.

3.1.3.4 Differential GPS

Differential GPS can be used in a limited area by assigning one reference position where a GPS receiver is located. The position error between the known position and the measured position is then used to compensate the calculated positions of GPS receivers in the same area. For the original 400km diameter of LOFAR this was not a viable solution and the Motorola chipset is set in a time-mode which is more accurate than the time+positioning mode and in time-mode it is not possible to use differential GPS as the position is already known. It could be an option to collect the information of the estimated propagation time from the GPS-satellites to the GPS receiver at CEP and estimate the error of the PPS at the different stations in retrospect.

3.1.3.5 Single satellite GPS

It is possible to use only one satellite from the GPS system as reference clock, thereby allowing for a significantly larger error towards UTC that with a normal GPS solution, however the error between different GPS receivers will be smaller. This solution will result in a discontinuity when switching between satellites and it also excludes the use of an Rb-reference because it will only track this discontinuity over a period of several hours

3.1.3.6 Other GPS receivers

The Motorola receivers were selected because they provided a very good accuracy at a reasonable price. Alternatives with a comparable performance were at the time of the investigation significantly more expensive.

3.1.3.7 Other Rb-reference standards

Other Rb-reference standards have been investigated, but the experience with the SRS-FS725 within ASTRON and in LOFAR has been positive and it's relatively cheap considering the specification compared to competitors. Also, the SRS-FS725 has aligned the outgoing PPS with the incoming PPS which is essential for the solution used in LOFAR. Measurements were performed on a combined GPS with Rb-reference from Fluke. With this unit, there is no predetermined relation between the incoming and the outgoing PPS; there is an unknown offset of between 0s and 1s. The unit was very sensitive to temperature changes. A change in temperature results in a time offset which is not recovered when the temperature returns.

3.2 Clock distribution within a station

Within a station, the PPS signal needs to be distributed to the LCU but also to the RSP boards as all commands from the LCU to the RSP boards are aligned with the PPS signal. Furthermore, the 10MHz of the Rb-reference needs to be up converted to 160/200MHz for the AD converter clocks and the FPGA clocks on the RSP boards.

3.2.1 Solution for LOFAR Stations

For the LOFAR Stations the same basic building blocks are used that were designed and tested for FTS. These consist of a programmable PLL for the 10MHz to 160MHz conversion, a second PLL for the 10MHz to 200MHz conversion and PECL clock buffers with 2 inputs and 10 outputs with low jitter.

The PPS from the Rb-reference is distributed to all six TDS boards in a station. On a TDS board, the incoming PPS is copied into 4 PPS signals and each PPS is distributed to an RSP board. The PPS is distributed over the backplane as LVTTL. The PPS is used by the LCU to schedule commands on the RSP boards and the PPS is also used to synchronise the data over the transport ring between RSP boards.

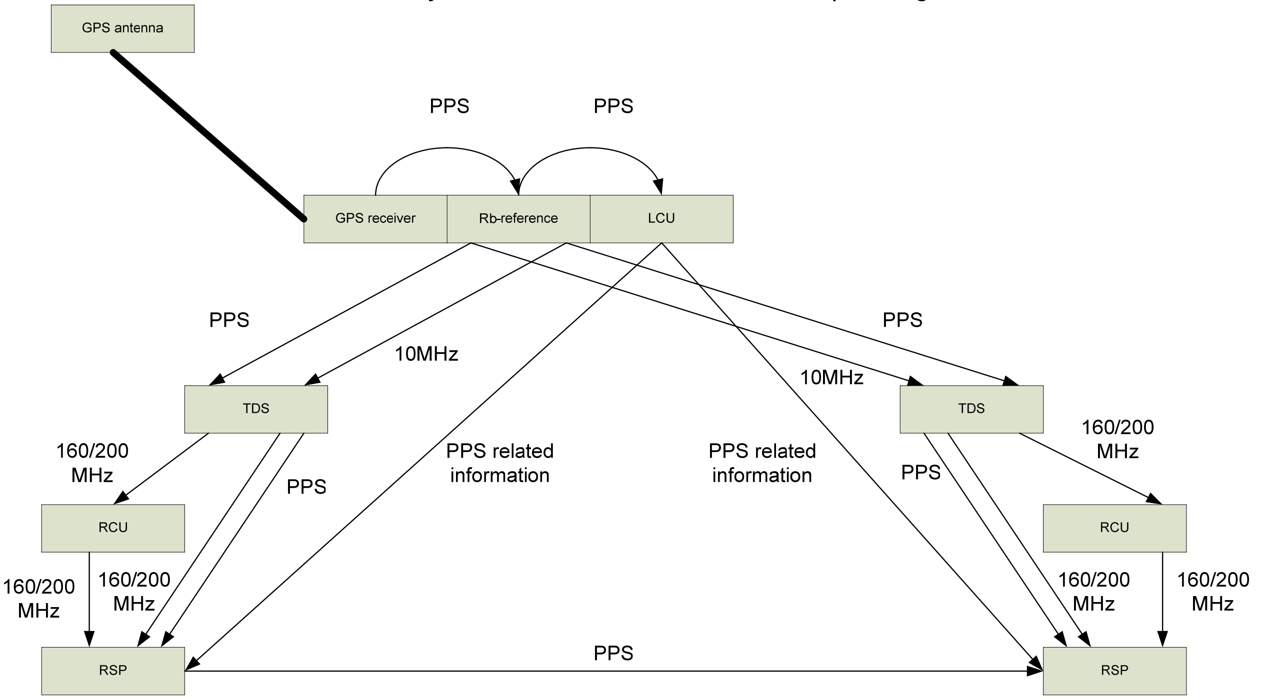

Figure 2, Distribution of the PPS and clock signals within a station

The 10MHz signal from the Rb-reference is also distributed to all six TDS boards in a station. The TDS boards can be configured to accept single ended or differential signals. On the TDS board there are two PLLs one for 200MHz and one for 160MHz and depending on the control settings, one of the two is used. Either the 160MHz or the 200MHz signal is than copied to 38 clock signals using PECL clock buffers. 32 LVPECL clock signals go to the RCU's in a subrack and the remaining LVPECL clock signals are distributed to the RSP and TBB boards. The 160MHz or 200MHz clock that is used by the AD converter on the RCU boards is send together with the digital data to the RSP board to allow the FPGAs on the RSP board to clock in the data from the AD converters.

The PLLs are based on a semi 'COTS' VCXO together with a PLL frequency synthesiser with a 1kHz loop filter. The resulting phase noise at 1kHz is -130dBc (simulated).
For the clock distribution between boards and for the generation of 192 clocks per station, LVPECL was chosen as a reference. LVPECL is a relatively mature standard for high speed data and clock distribution systems which is supported by different chip-suppliers. The components used generate a typical random clock jitter of 0.2ps RMS.

The TDS board is provided with +48V from the backplane. Using a DC/DC converter, +5V is created which is reduced to +3.3V power plane using linear regulators to provide the low noise power for the circuitry on the TDS board. DC/DC converters are renowned for the electromagnetic radiation they generate and some measures have been taken to compensate for this. To minimize disturbances on the 3.3V lines, the 3.3V is split in separate regions, 160MHz block, 200MHz block and the Clock and PPS tree.

3.2.2 Other investigated alternatives

3.2.2.1 VCXOs with a PECL output

The current supplier of VCXOs (Valpey Fisher) has an option to provide them with a PECL output instead of the single ended output used today. The performance in terms of jitter and phase noise for the version with a PECL output is significantly worse and therefore this option is not used.

3.2.2.2 Alternative PLL synthesiser chips

Several alternatives have been investigated however at the time; the ADF4107 introduced the least noise. During the design other, promising chips were spotted but for lead time reasons these have not been evaluated or included in the design.

3.2.2.3 Analogue clock distribution

An alternative would have been to generate a single high power sine wave as a reference clock and distribute this to all RCU's using a high power amplifier (PA) and a series of splitters. To keep the signal linear, a PA with a rather large power rating (1dB compression point 1-10kW) would have to be developed unless the PA would be enhanced with advanced linearization techniques.

3.2.2.4 TTL/LVTTL

Other types of transmission standards have also been investigated to a limited extend, however no 1:n clock buffer chips with better performance could be found. An LVDS based solution might prove a viable alternative at some point in the future.

3.2.2.5 Rb-Reference to TDS interface

There are several ways to implement this interface. Because the Rb-reference only supports single ended coax outputs at this time, the interface to the TDS board has been designed single ended coax. When EMC problems occur this interface can be updated to a differential interface using infiniband cabling.

3.3 Control Architecture

From a larger perspective, also the clock system is controlled centrally from the CCU however for the purpose of this document; it is assumed that the LCU controls the clock subsystem.

3.3.1 Control Architecture

The different control interfaces for the SCO are described in Figure 3. The GPS receiver and the Rb-reference standard are controlled via RS-232. The TDS boards are connected via I2C to the RSP board. The TDS board can be controlled either directly from the RSP board or from the LCU, via Ethernet to the RSP board. The Control interface is described in detail in [5].

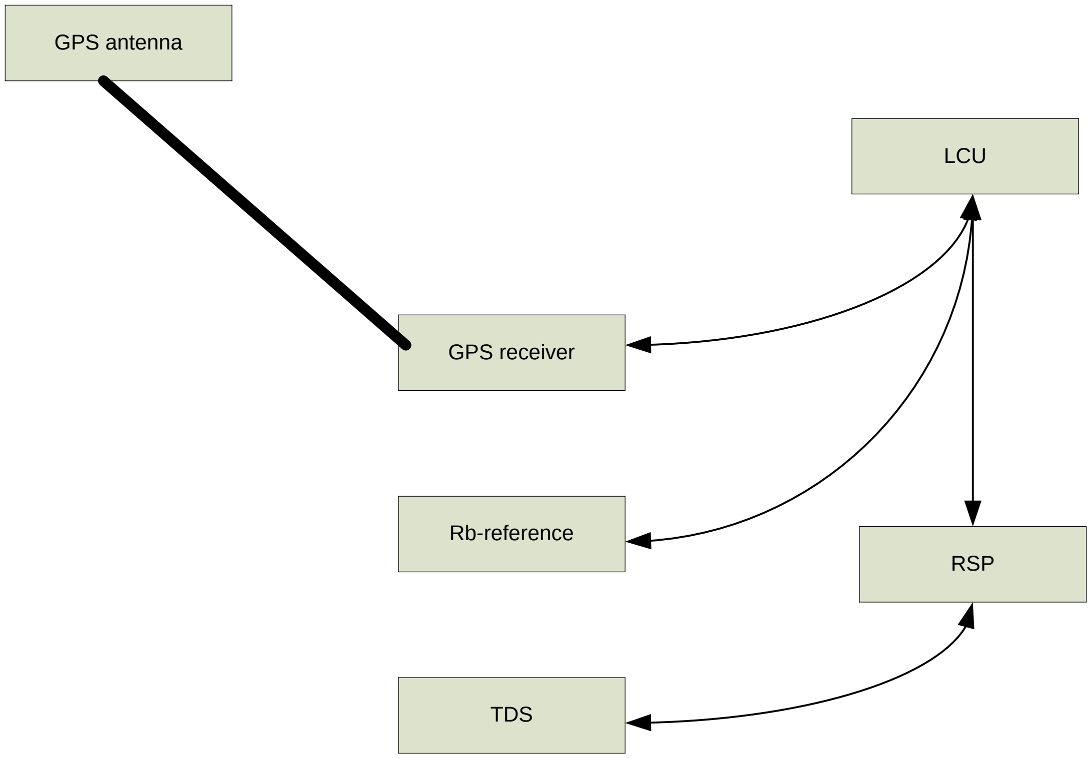

Figure 3, Control interfaces relevant to the SCO subsystem

The GPS receiver needs to be configured during the commissioning of a LOFAR station and these initial configuration data is stored in flash memory on the GPS receiver. After a restart or reset, the stored configuration will be reloaded. The GPS receiver is also capable of checking the GPS antenna.

The Rb-reference needs to be reprogrammed during commissioning. After each restart or reset default values, stored during commissioning, will be loaded into the Rb-reference.

The TDS board always starts up at 200MHz even though the PLL will not be locked. The RSP boards can start up using the 200MHz, after which the TDS board can be programmed by the RSP board. As 4 RSP boards are connected to 1 TDS board via an I2C interface, the LCU will select one RSP board for programming the TDS board.

Each unit in the clock system can provide status information upon request to the LCU. A minimum set of support commands are listed in [5]. The manuals of the GPS receiver and the Rb-reference see [7], provide information over additional commands.

4 Clock Measurement Results

In this section the measurement done in May 2005, prior to the selection of the test system in Exloo, are described. The measurements were done by Sieds Damstra and André van Houwelingen.

4.1 Inter Station measurements

All interstation measurements have been performed using the PPS signal of either a GPS receiver or an Rb-reference standard as the measurement setup was not capable of performing automatic measurements on the 10MHz signals from the Rb-reference standards. A manual Allan Variance measurement using the 10MHz signals confirmed that they were more slightly more stable than the 1PPS signals. A measurement with FTS-1 configured as two remote stations, each with its own GPS/Rb-reference is planned but has not been done so far.

4.1.1 GPS vs. GPS measurements

In this setup the PPS signals from both GPS receivers are fed into the time interval counter. One of the PPS signals is delayed by inserting a 20m cable to make sure that one PPS signal can be used as a trigger and the time until the arrival of the second PPS signal is measured. The measurement was done during a 2.5 day period (a weekend).

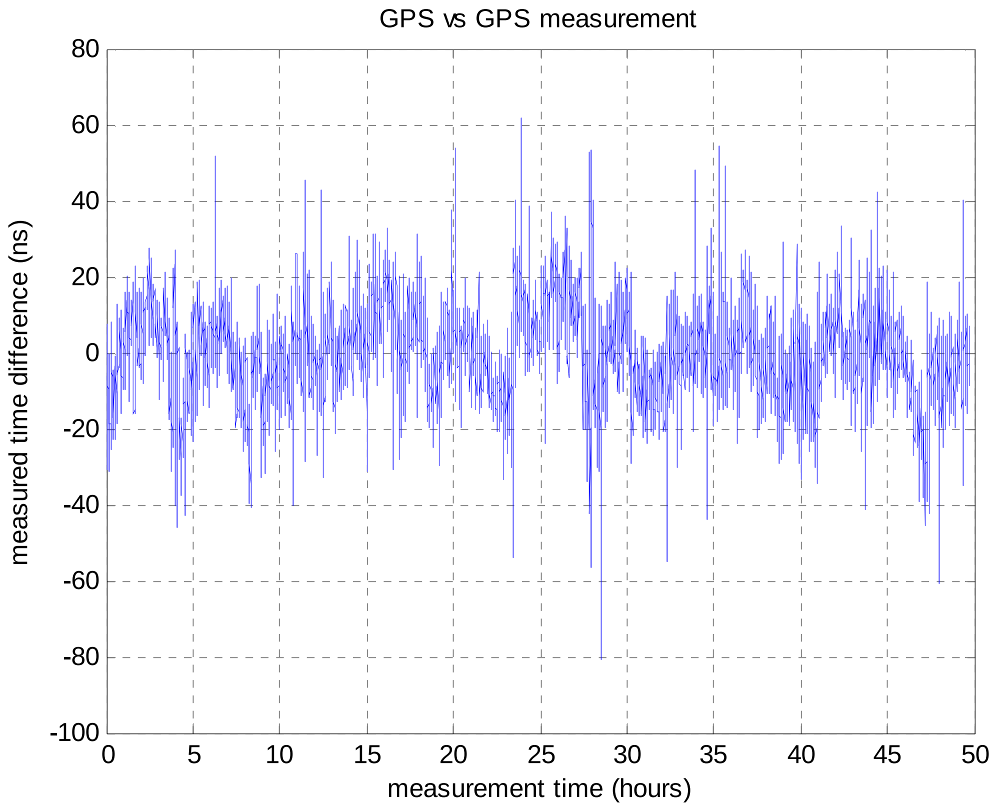

Figure 4, Measurement result of a time difference measurement between the PPS signals of two GPS receivers

No visible effect of the atmospheric and temperature changes can be seen. As can be seen in Figure 4, a maximum offset of 80ns is reached at one point. The RMS offset is 11ns when measured against each other. Assuming that both GPS receivers have the same characteristics, it can be estimated that the offset of one

GPS receiver to UTC is in the order of8ns. According to the specification, the RMS offset towards UTS should be 10ns. So the GPS receivers comply with this specification.

4.1.2 GPS vs. Rb-reference slaved to GPS

In this measurement, the Rb-reference clock is significantly more stable than a GPS receiver over a time period of several hours. The Rb-reference is slaved to a 2nd GPS receiver to provide long term stability. Measurements performed on Motorola M12 chipsets versus a Maser reference clock which were done and published by CNS showed a strange behaviour of the Motorola 1pps signal [6]

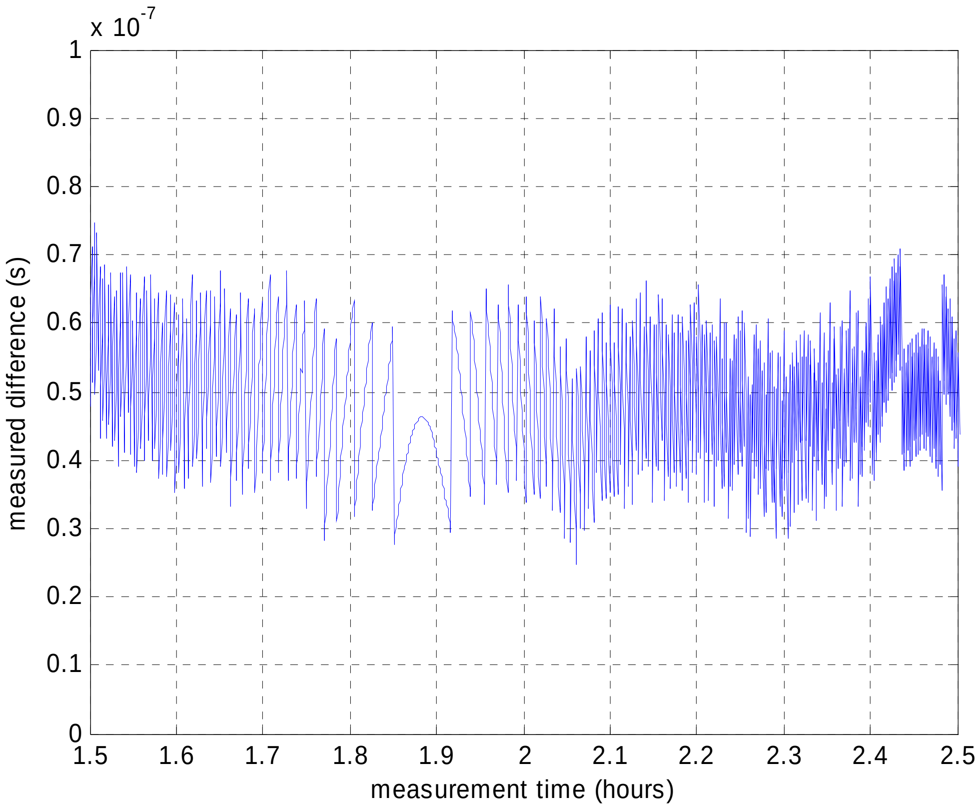

Figure 5, Measured time difference for a measurement between a GPS receiver and an Rb-reference clock slaved to a second GPS receiver.

In Figure 5 it can be seen that the same strange behaviour is also present in the measurements performed here, which is shows that the test setup performs very well. The variation visible on the measurement data is according to CNS caused by the 16.367MHz sample clock used in the GPS receiver. The Motorola has an option on the control interface to read out with the clock granularity message an estimate on how much earlier or later the PPS signal is given. Using this information the PPS accuracy could be improved to an RMS value of:2ns according to specification.

4.1.3 Rb-reference vs. Rb-reference measurements, both slaved to GPS

In this measurement setup, 2 Rb references where used. Each Rb reference was slaved to its own GPS receiver. The result is shown in Figure 6. It is assumed that the drift seen in Figure 6 is the result of temperature variations at the measurement site as the temperature inside 'huisje west' easily changed 15° over a day/night cycle. The RMS offset to UTC, again assuming 2 clock systems with the same accuracy, is

2.5ns which is very close to the 2ns specification of the GPS receiver when using the clock granularity message.

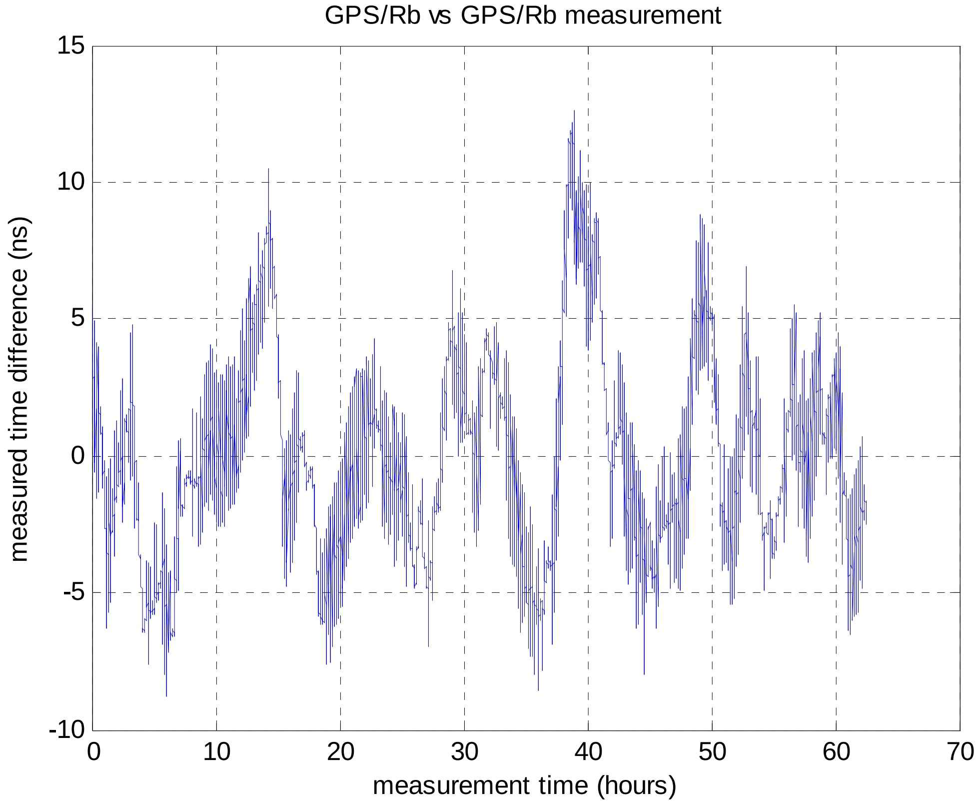

Figure 6, GPS with Rb-reference vs. GPS with Rb-reference measurement over a weekend

4.1.4 Measurements with Fluke vs. SRS FS725

A from Fluke 910R was available for testing and several measurements have been performed, comparing this unit with the Stanford Research Systems FS725. The Fluke has a build in GPS receiver and for the SRS FS725, the Motorola M12+ was used. Measurements were performed with the SR620 to determine the performance of these two time standards. One problem with the Fluke 910R is, is that the output PPS is derived from the output 10MHz but there is no control over the offset between the input and output PPS and thus the offset is somewhere between -0.5 and +0.5s determined by the start-up moment of the Fluke. By trial and error, the PPS was aligned somewhat with the PPS from the FS725 and a long measurement was performed. The result is shown in Figure 7.

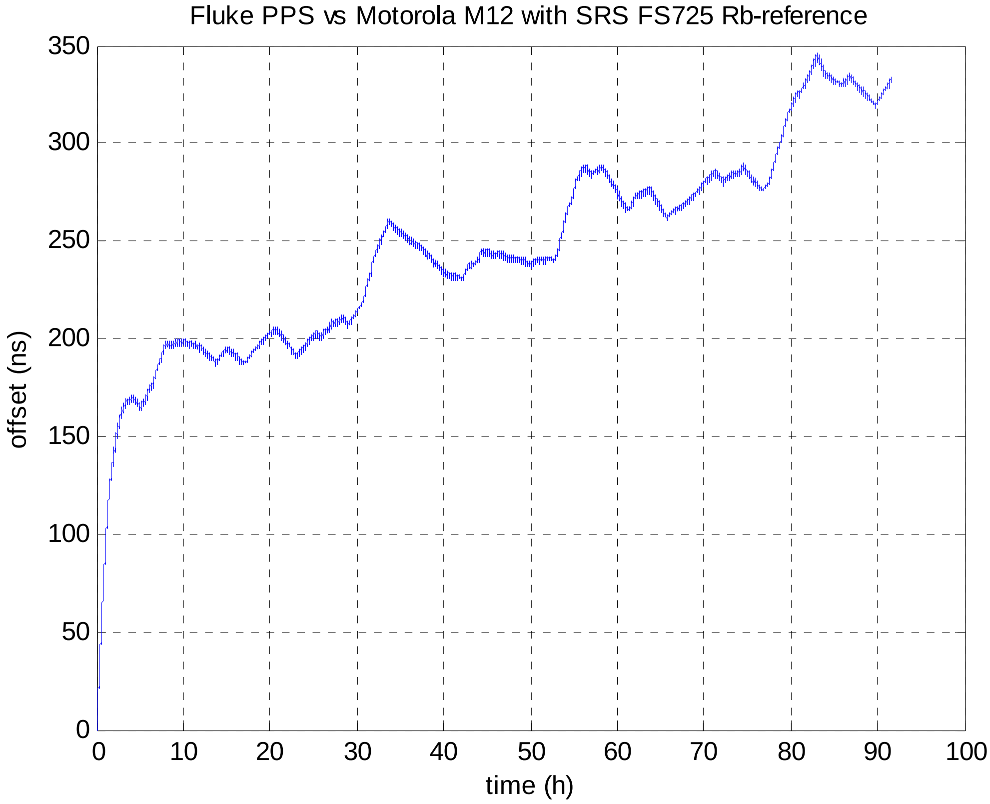

Figure 7, Measurement result between the Fluke and the SRS Rb-references

As can be seen, the two reference drift apart, even though both are locked to GPS during the measurement. The strong drift in the beginning is caused by the start-up behaviour of the Fluke. After the initial start-up, the Fluke drifts away from the FS725, where there is a strong correlation with the environment temperature. The drift is also permanent, in contrast with measurements performed between two FS725's were drift is counteracted by the influence of the GPS receivers.

This effect in the Fluke equipment has been verified with the production organization that produces this equipment for Fluke and they are aware of this behaviour. They realized that this behaviour made the unit unsuitable for astronomical application and they were willing to change this behaviour but this would take a minimum of 6months lead-time and was therefore outside the scope of the evaluation.

4.2 Intra Station measurements

The intra station measurements is an area where measurements are still ongoing on FTS-1. The measurements performed up to the review of this document are described in the following paragraphs. Other measurements are planned and when results become available, they will be added in a new revision of this document.

4.2.1 Clock board measurement using the Agilent 86100B Wide bandwidth Oscilloscope

These measurements were performed on three different clock boards on both 160 and 200MHz. The 86100B is specified with a characteristic jitter of 1ps RMS when using a direct trigger. Both the measured and the trigger signal were taken from the same clock board. For the 160/200MHz signals, for the 3 clock boards and different output port combinations measurements were performed and an example of the result is shown in Figure 8.

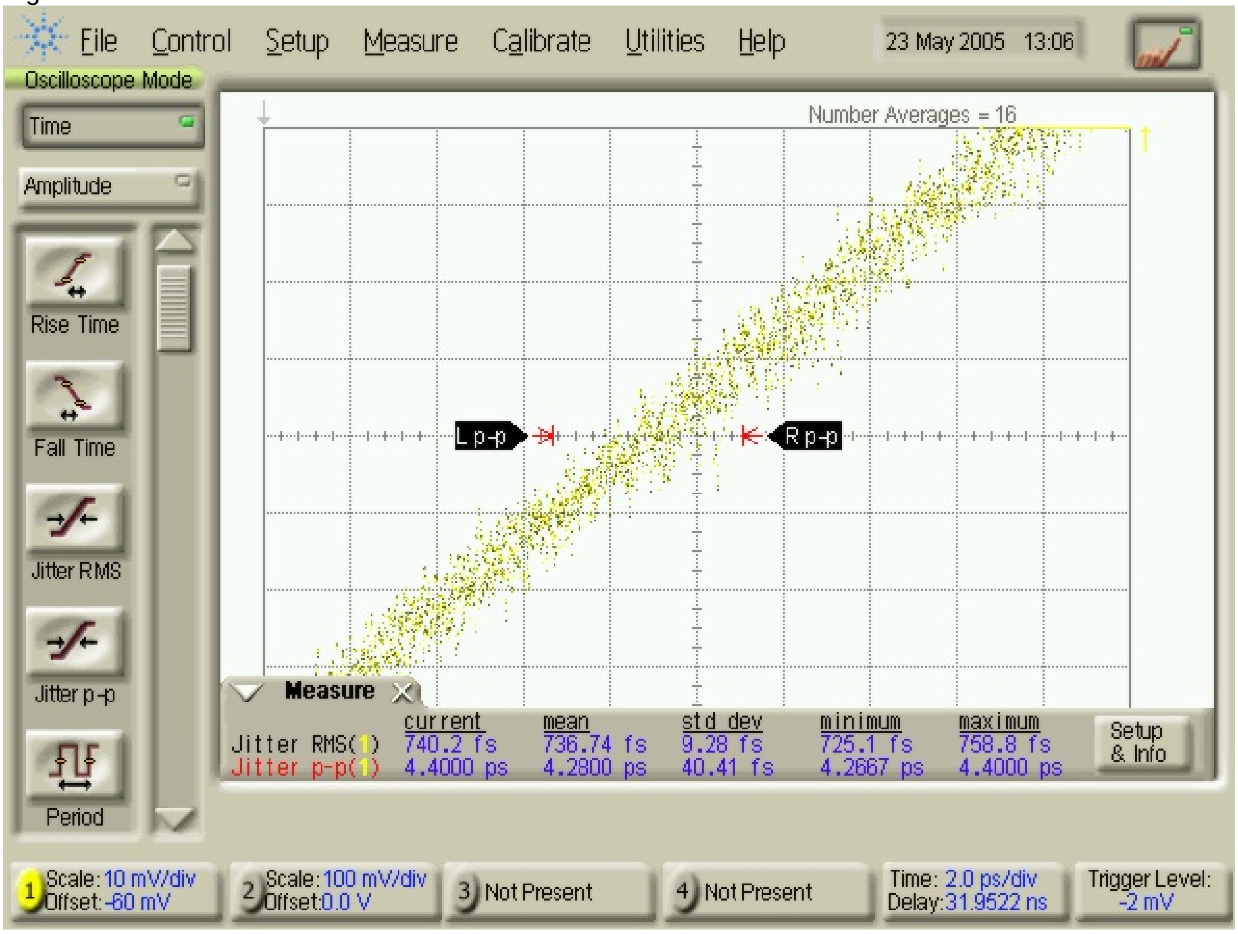

Figure 8, jitter measurement of a clock board using the Agilent 86100B

4.2.2 Clock measurements using LOFAR FTS-1

Using the LOFAR FTS-1 hardware as an under sampling scope, the difference between the sample time between two RCU's connected to the backplane clock were measured and the result is shown in Figure 9. Though difficult to see in the graph, the RMS difference between the clock signals is 350fs

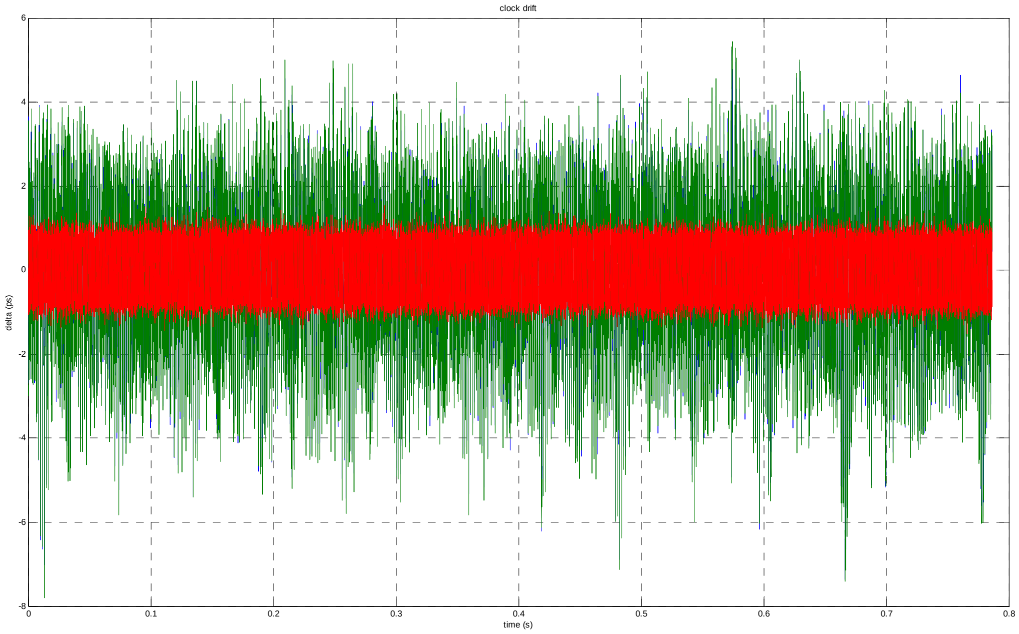

Figure 9, jitter measurement using LOFAR FTS-1 as an under sampling scope